



PSMN5R6-100BS

N-channel 100 V 5.6 mΩ standard level MOSFET in D2PAK

Rev. 1 — 20 March 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in a SOT404 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

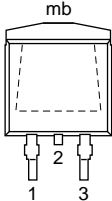
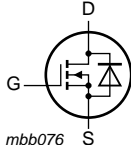
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--|--|-----|------|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | - | 100 | V |
| I_D | drain current | $T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 | [1] | - | 100 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C};$ see Figure 2 | - | - | 306 | W |
| T_j | junction temperature | | -55 | - | 175 | °C |
| Static characteristics | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 100\text{ °C};$ see Figure 12 ; see Figure 13 | - | 8.5 | 10 | mΩ |
| | | $V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ see Figure 13 | - | 4.72 | 5.6 | mΩ |
| Dynamic characteristics | | | | | | |
| Q_{GD} | gate-drain charge | $V_{GS} = 10\text{ V}; I_D = 25\text{ A}; V_{DS} = 50\text{ V};$ see Figure 14 ; see Figure 15 | - | 43 | - | nC |
| $Q_{G(tot)}$ | total gate charge | | - | 141 | - | nC |
| Avalanche Ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ $I_D = 100\text{ A}; V_{sup} \leq 100\text{ V};$ $R_{GS} = 50\text{ Ω};$ unclamped | - | - | 468 | mJ |

[1] Continuous current limited by package.



2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|---|---|
| 1 | G | gate |  <p>SOT404 (D2PAK)</p> |  |
| 2 | D | drain ^[1] | | |
| 3 | S | source | | |
| mb | D | mounting base; connected to drain | | |

[1] It is not possible to make connection to pin 2

3. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|---------------|---------|--|---------|
| | Name | Description | Version |
| PSMN5R6-100BS | D2PAK | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404 |

4. Marking

Table 4. Marking codes

| Type number | Marking code |
|---------------|---------------|
| PSMN5R6-100BS | PSMN5R6-100BS |

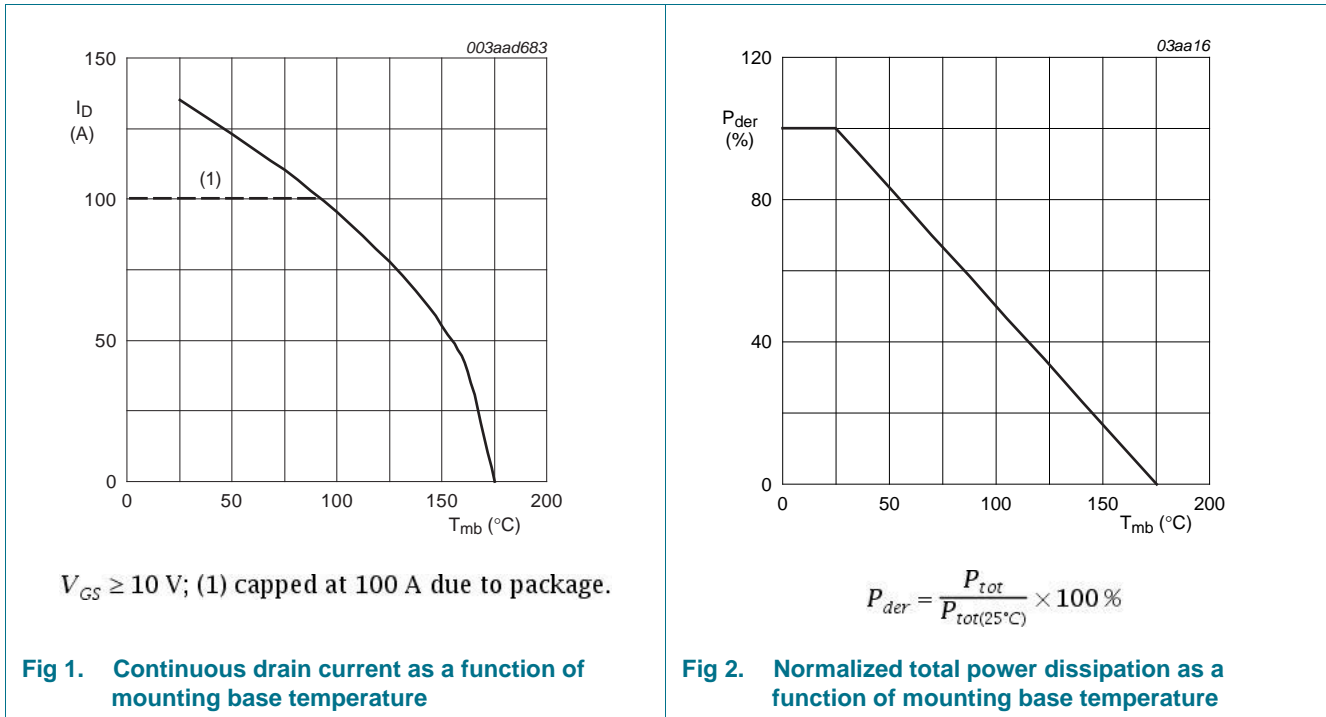
5. Limiting values

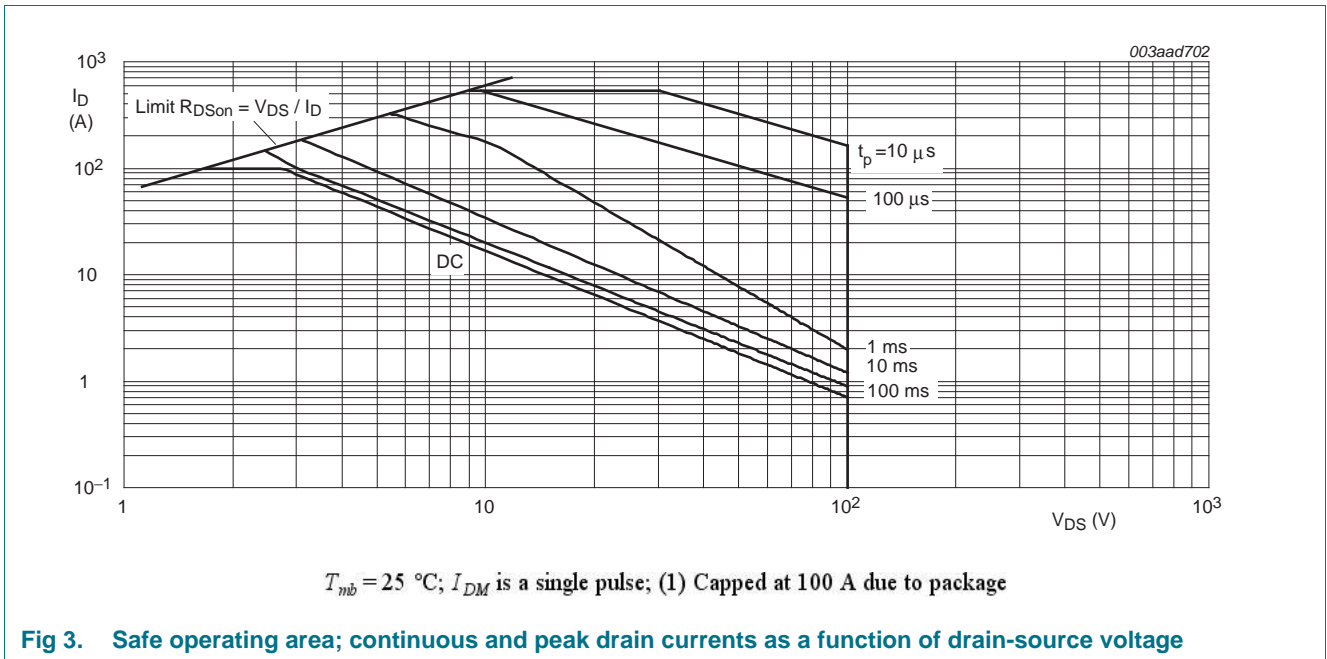
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|--|---|-----|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | 100 | V |
| V_{DGR} | drain-gate voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$ | - | 100 | V |
| V_{GS} | gate-source voltage | | -20 | 20 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}; T_j = 100\text{ °C}$; see Figure 1 | - | 95 | A |
| | | $V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$; see Figure 1 [1] | - | 100 | A |
| I_{DM} | peak drain current | pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3 | - | 539 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; see Figure 2 | - | 306 | W |
| T_{stg} | storage temperature | | -55 | 175 | °C |
| T_j | junction temperature | | -55 | 175 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | - | 260 | °C |
| Source-drain diode | | | | | |
| I_S | source current | $T_{mb} = 25\text{ °C}$ | [1] | 100 | A |
| I_{SM} | peak source current | pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$ | - | 539 | A |
| Avalanche Ruggedness | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 100\text{ A}; V_{sup} \leq 100\text{ V}; R_{GS} = 50\text{ }\Omega$; unclamped | - | 468 | mJ |

[1] Continuous current limited by package.





6. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|---|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | 0.3 | 0.49 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Minimum footprint; mounted on a printed circuit board | - | 50 | - | K/W |

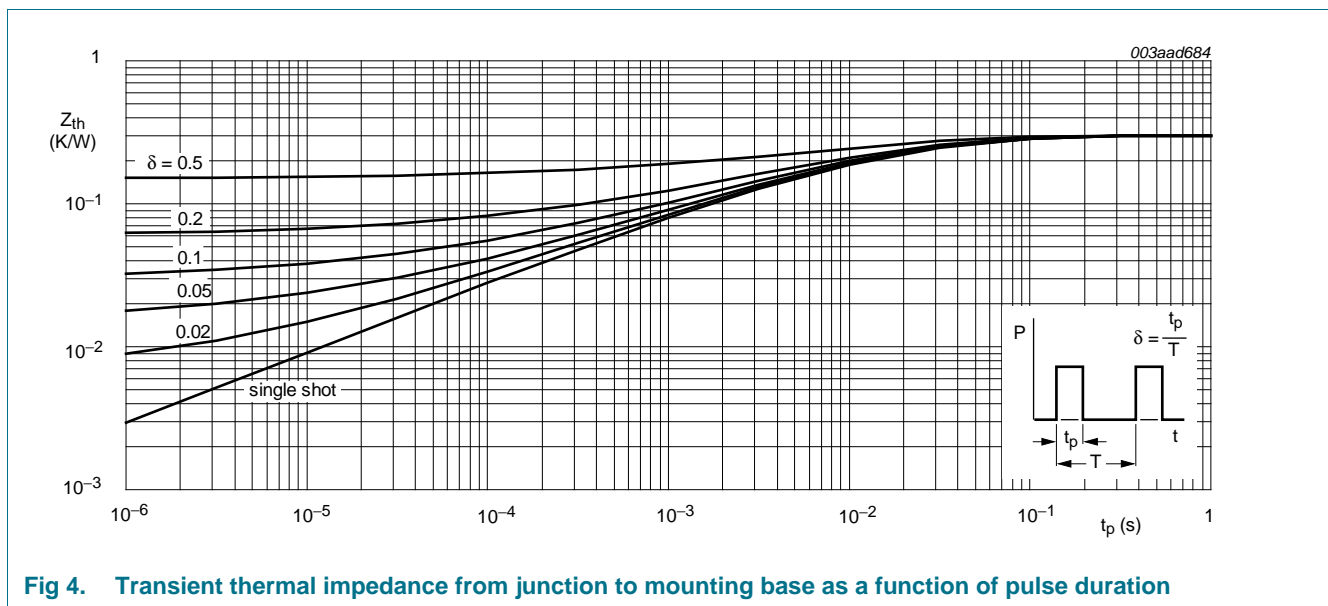


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

7. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------|---|-----|-------|------|---------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | 100 | - | - | V |
| | | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$ | 90 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 10 ; see Figure 11 | 2 | 3 | 4 | V |
| V_{GSth} | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 11 | 1 | - | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 11 | - | - | 4.6 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 0.02 | 10 | μA |
| | | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$ | - | - | 500 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 10 | 100 | nA |
| | | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 10 | 100 | nA |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13 | - | 8.5 | 10 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13 | - | 13.22 | 15.5 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 13 | - | 4.72 | 5.6 | mΩ |
| R_G | gate resistance | $f = 1 \text{ MHz}$ | - | 0.97 | - | Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15 | - | 141 | - | nC |
| | | $I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$ | - | 130 | - | nC |
| Q_{GS} | gate-source charge | $I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15 | - | 36 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | - | 22 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | - | 14 | - | nC |
| Q_{GD} | gate-drain charge | | - | 43 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D = 25 \text{ A}; V_{DS} = 50 \text{ V};$ see Figure 14 ; see Figure 15 | - | 4.9 | - | V |
| C_{iss} | input capacitance | $V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 16 | - | 8061 | - | pF |
| C_{oss} | output capacitance | | - | 561 | - | pF |
| C_{riss} | reverse transfer capacitance | | - | 330 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 50 \text{ V}; R_L = 0.6 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 1.5 \text{ } \Omega$ | - | 31 | - | ns |
| t_r | rise time | | - | 46 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 83 | - | ns |
| t_f | fall time | | - | 34 | - | ns |

Table 7. Characteristics ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|-----------------------|--|-----|------|-----|------|
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17 | - | 0.79 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; | - | 67 | - | ns |
| Q_r | recovered charge | $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$ | - | 182 | - | nC |

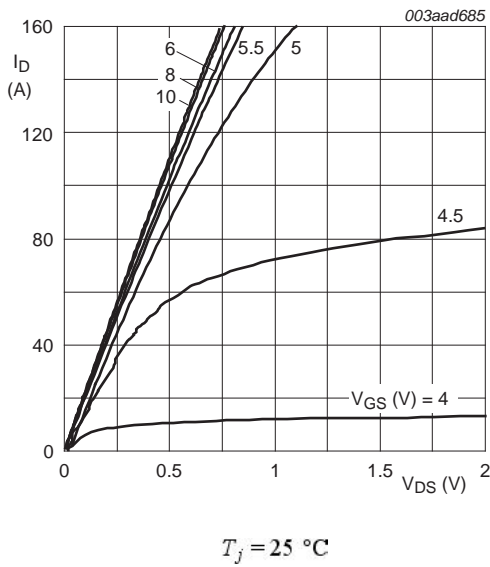


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

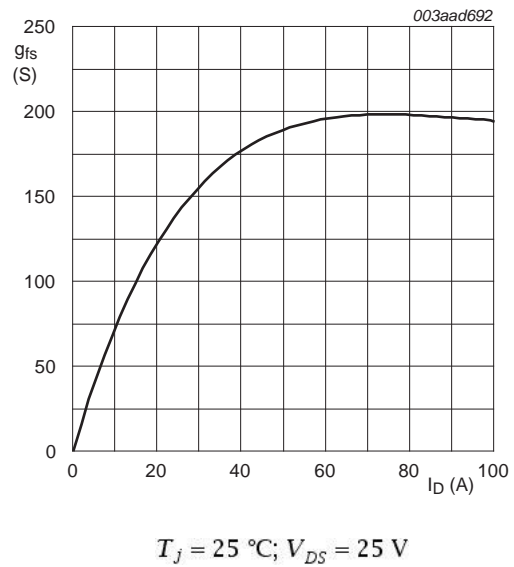


Fig 6. Forward transconductance as a function of drain current; typical values

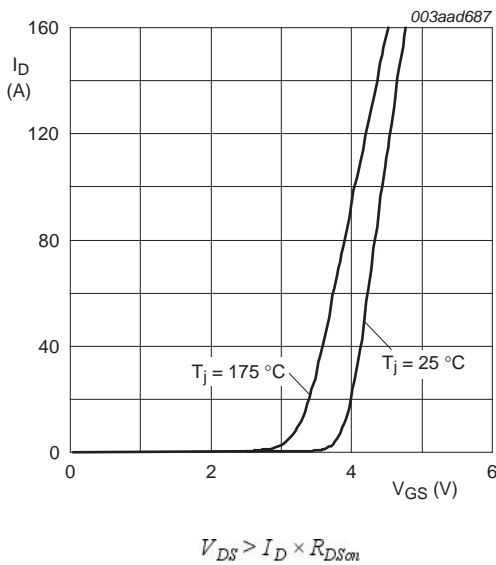


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

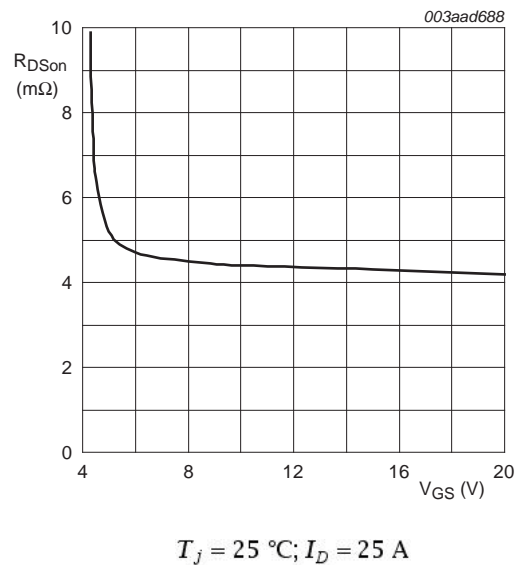
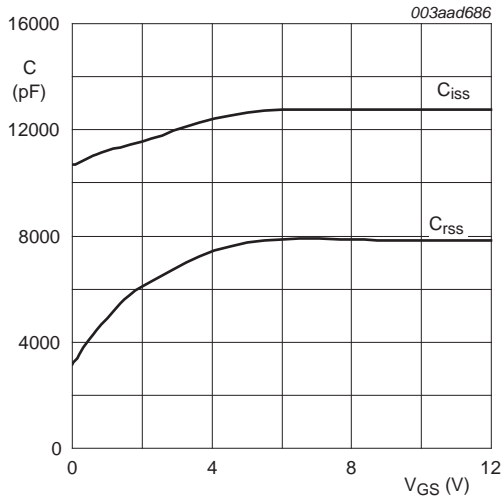
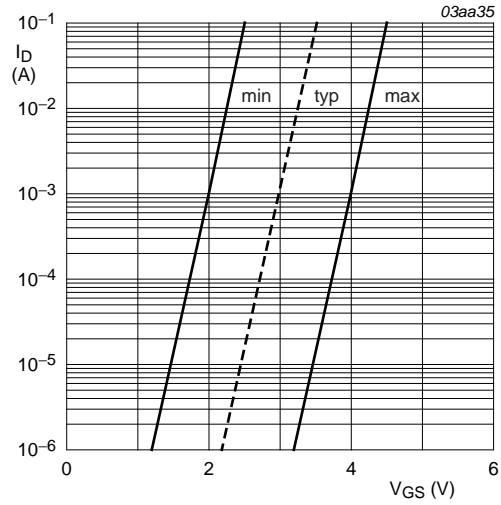


Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



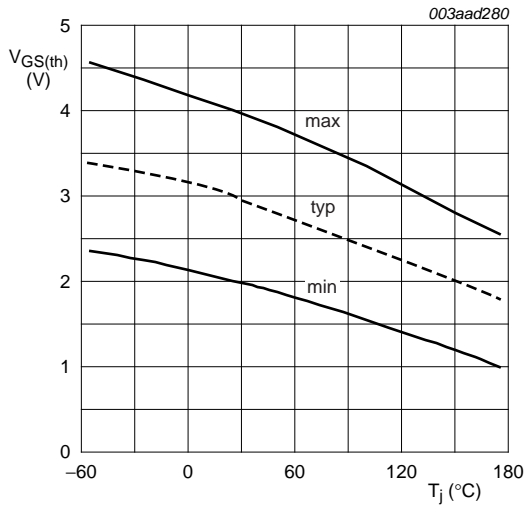
$f = 1 \text{ MHz}; V_{DS} = 0 \text{ V};$

Fig 9. Input and reverse transfer capacitances as a function of gate-source voltage, typical values



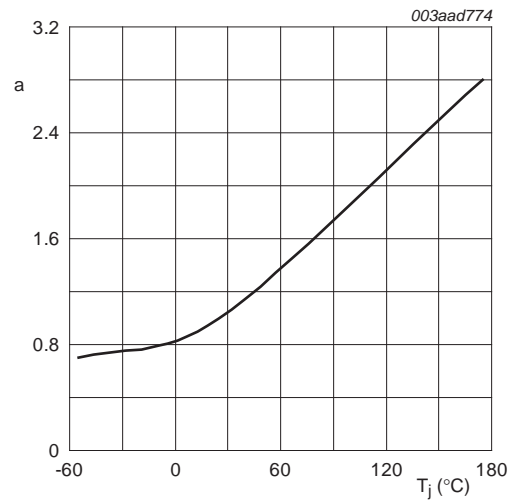
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DS(on)}}{R_{DS(on)25^\circ\text{C}}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

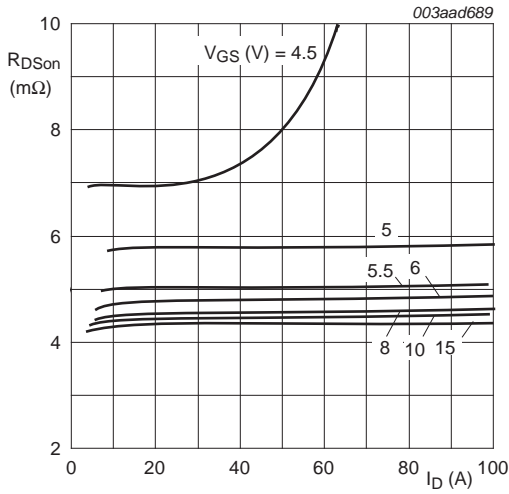


Fig 13. Drain-source on-state resistance as a function of drain current; typical values

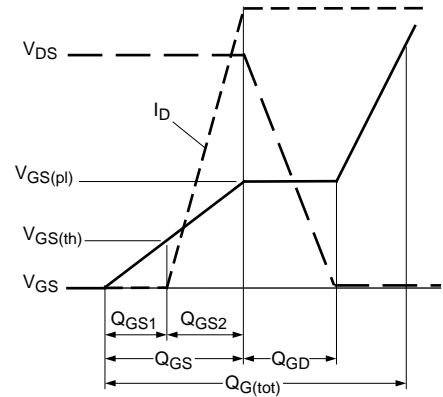


Fig 14. Gate charge waveform definitions

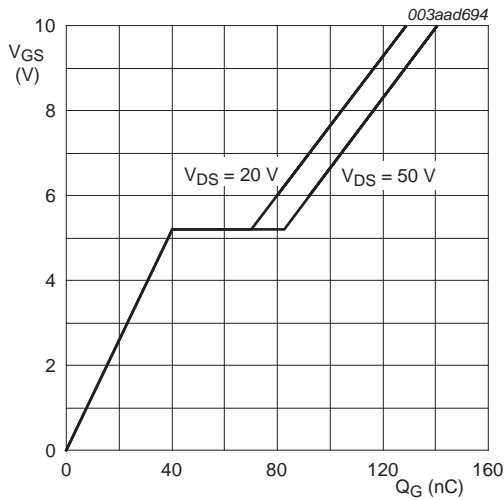


Fig 15. Gate-source voltage as a function of gate charge; typical values

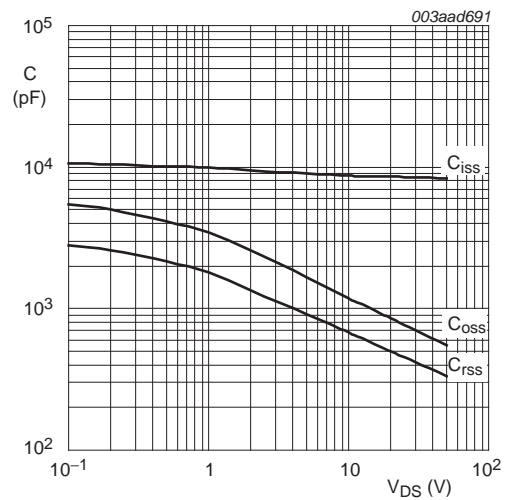


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

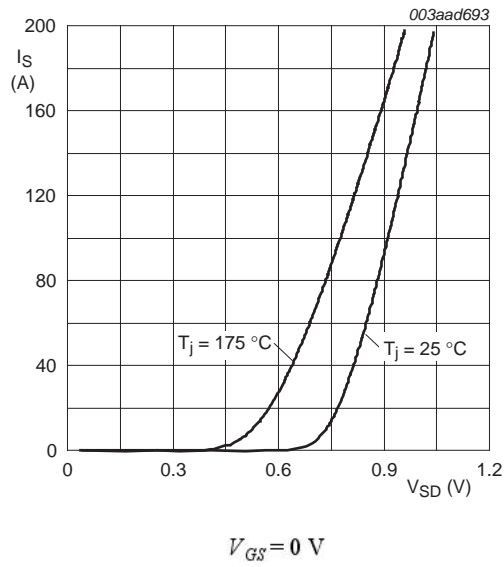


Fig 17. Source current as a function of source-drain voltage; typical values

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

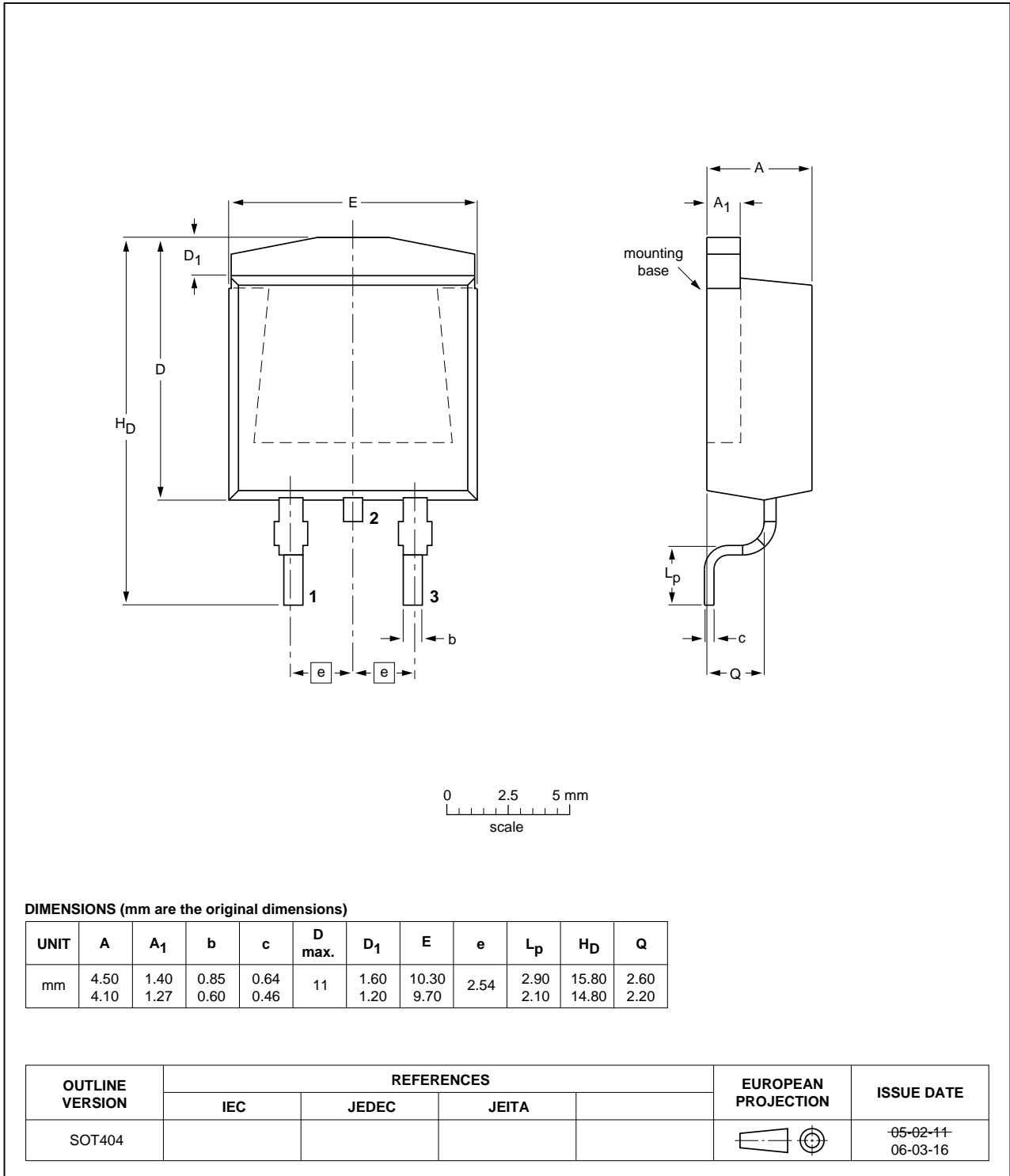


Fig 18. Package outline SOT404 (D2PAK)

9. Revision history

Table 8. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|--------------|--------------------|---------------|------------|
| PSMN5R6-100BS v.1 | 20120320 | Product data sheet | - | - |

10. Legal information

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|------------------------------------|-------------------------------|---|
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